I CLAIM:

1. A method of deactivating a word line in a memory circuit, said method comprising:

activating a plurality of word lines either one at a time, simultaneously in subpluralities, combinations thereof, or all simultaneously, all said word lines being active concurrently; and

deactivating one of said word lines, the other of said word lines remaining active.

2. The method of claim 1 further comprising enabling said one of said word lines before said deactivating.

3. The method of claim 1 wherein said deactivating comprises deactivating one of said word lines in response to receiving a signal pulse, the other of said word lines remaining active, other pulses of said signal used to activate said word lines.

4. A method of deactivating a word line in a memory circuit, said method comprising:

receiving a first pulse of a signal;

activating a word line in response to said receiving a first pulse;

receiving a subsequent pulse of said signal, said subsequent pulse having the same logical value as said first pulse; and

deactivating said word line in response to said receiving a subsequent pulse.

5. The method of claim 4 further comprising generating pulses of said signal to activate enabled word lines.

6. The method of claim 4 further comprising enabling activation of said word line before said receiving a first pulse.

7. The method of claim 4 further comprising enabling deactivation of said word line before said receiving a subsequent pulse.

8. The method of claim 4 further comprising after said deactivating:

receiving a second subsequent pulse of said signal; and

activating said word line in response to said receiving a second subsequent pulse.

9. The method of claim 4 further comprising:

receiving a second signal; and

deactivating all activated word lines in response to said receiving a second signal.

10. A method of deactivating a word line in a memory circuit, said method comprising:

deactivating all word lines in said memory in response to receiving a first signal;

activating a word line in response to receiving a second signal and a pulse of a third signal; and

deactivating only said word line in response to receiving said second signal, a fourth signal, and a subsequent pulse of said third signal, said pulse and said subsequent pulse having the same logical value.

11. The method of claim 10 further comprising reactivating only said word line in response to receiving said second signal, a fourth signal, and a second subsequent pulse of said third signal.

12. The method of claim 10 wherein said first signal is a precharge signal.

13. The method of claim 10 wherein said second signal is an address signal.

14. The method of claim 10 wherein said third signal is an activate word line signal.

15. The method of claim 10 wherein said fourth signal is a deactivate enable signal.

16. A method of deactivating less than all activated memory word lines in a memory circuit, said method comprising:

receiving at least one pulse of a signal;

activating a plurality of word lines in response to said receiving at least one pulse;

selecting a subplurality of said word lines to be deactivated;

receiving a subsequent pulse of said signal; and

deactivating said subplurality of word lines in response to said receiving a subsequent pulse.

17. A method of deactivating a single memory word line among a plurality of activated word lines in a memory circuit, said method comprising:

receiving a plurality of address signals;

receiving at least one activate signal pulse;

activating a plurality of word lines corresponding respectively to said plurality of address signals in response to said receiving at least one activate signal pulse;

receiving one of said plurality of address signals after said activating;

receiving a deactivate enable signal corresponding to said one address signal;

receiving a subsequent activate signal pulse after said activating; and

deactivating only said word line corresponding to said one address signal in response to said receiving a subsequent activate signal pulse.

18. A method of deactivating a single memory word line among a plurality of activated word lines in a memory circuit, said method comprising:

generating a sequential series of signal pulses, each said pulse operative to activate a word line and having the same logical value;

activating a plurality of word lines either simultaneously, sequentially, or in combinations thereof in response to said signal pulses;

selecting one of said active word lines; and

deactivating only said one selected word line in response to one of said signal pulses.

19. A memory circuit comprising:

a first input node operative to receive a precharge signal;

a second input node operative to receive a word line activate signal;

a third input node operative to receive an address signal;

an output node operative to provide a signal indicating whether a word line is to be activated or deactivated;

a first switch controlled by said precharge signal and having a first node coupled to a first voltage and having a second node;

a second switch controlled by said activate signal and having a first node operative to receive said address signal and having a second node;

a third switch coupled between said first switch second node and said second switch second node;

a fourth switch having a first node coupled to a second voltage and a second node coupled to said first switch second node;

at least one signal driver element coupled between said first switch second node and said output node;

a delay element coupled to receive a signal derived from said address signal and outputting a signal that controls said third switch; and

a logic gate coupled to receive said activate and address signals, said delay element output signal, and an enable signal, said logic gate outputting a signal that controls said fourth switch.

20. The circuit of claim 19 wherein said first voltage and second voltage are the same.

21. The circuit of claim 19 wherein said first, second, third, and fourth switches each comprise a transistor.

22. The circuit of claim 19 wherein each said transistor is a field-effect-transistor.

23. The circuit of claim 19 wherein said first and fourth switches each comprise a p-channel metal-oxide-semiconductor field-effect-transistor.

24. The circuit of claim 19 wherein said second and third switches each comprise an n-channel metal-oxide-semiconductor field-effect-transistor.

25. The circuit of claim 19 wherein said logic gate comprises a NOR gate.

26. The circuit of claim 19 wherein said at least one signal driver element comprises an inverter.

27. The circuit of claim 19 wherein said at least one signal driver element comprises an odd number of inverters coupled in series between said first switch second node and said output node.

28. A system comprising:

a processor;

a memory controller coupled to said processor; and

a memory chip coupled to said memory controller, said memory chip comprising an array of memory cells, word lines, address decoder logic, and a latch circuit that outputs a signal indicating activation of a word line in response to receiving a first signal pulse of an activate signal and that outputs a signal indicating deactivation of said word line in response to receiving a deactivate-enable signal and a subsequent signal pulse of said activate signal.

29. The system of claim 28 wherein said memory chip comprises a dynamic random access memory.

30. The system of claim 28 wherein said latch comprises:

a first input node operative to receive a precharge signal;

a second input node operative to receive a word line activate signal;

a third input node operative to receive an address signal;

an output node operative to provide a signal indicating whether a word line is to be activated or deactivated;

a first switch controlled by said precharge signal and having a first node coupled to a first voltage and having a second node;

a second switch controlled by said activate signal and having a first node operative to receive said address signal and having a second node;

a third switch coupled between said first switch second node and said second switch second node;

a fourth switch having a first node coupled to a second voltage and a second node coupled to said first switch second node;

at least one signal driver element coupled between said first switch second node and said output node;

a delay element coupled to receive a signal derived from said address signal and outputting a signal that controls said third switch; and

a logic gate coupled to receive said activate and address signals, said delay element output signal, and an enable signal, said logic gate outputting a signal that controls said fourth switch.

31. The system of claim 30 wherein said first voltage and second voltage are the same.

32. Integrated circuit memory apparatus comprising:

means for deactivating all word lines in response to receiving a first signal;

means for activating a word line in response to receiving a second signal and a pulse of a third signal; and

means for deactivating only said word

line in response to receiving said second signal, a fourth signal, and a subsequent pulse of said third signal, said subsequent pulse having the same logical value as said pulse.

33. The apparatus of claim 32 further comprising means for reactivating only said word line in response to receiving said second signal, a fourth signal, and a second subsequent pulse of said third signal, said second subsequent pulse having the same logical value as said subsequent pulse.